Docket No.: 50090-309

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Yasuhito SUZUKI, et al.	:	
Serial No.: 09/915,366	:	Group Art Unit: 2811
Filed: July 27, 2001	:	Examiner: Quang D. Vu

For: SEMICONDUCTOR PACKAGE AND SEMICONDUCTOR DEVICE

REQUEST FOR RECONSIDERATION UNDER 37 C.F.R. 1.111

Commissioner for Patents
Washington, DC 20231

Sir:

In response to the December 31, 2002 non-final Office Action, reconsideration of the above-identified application is respectfully requested. Claims 1-13 are pending.

The Office Action has not acknowledged Applicants' claim of foreign priority. Accordingly, Applicants again respectfully bring the Examiner's attention to the Claim of Priority and Transmittal of Certified Priority Document submitted with the filing of this application on July 27, 2001 and request appropriate acknowledgement.

The Office Action rejects claims 1, 2 and 4 under 35 U.S.C. §102(b) over Ohki et al. (U.S. Patent No. 5,886,408), and further rejects claims 3 and 5-13 under 35 U.S.C. §103(a) over Ohki. These rejections are respectfully traversed.

In particular, Applicants assert that Ohki does not teach or suggest, or otherwise make obvious, a semiconductor device having outer leads that include upper electrical connecting surfaces on the side of the upper surface of a sealing member, and a lower electrical connecting surfaces on the side of the lower surface of the sealing member, respectively, and where the outer

leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of the sealing member from the same plane, as recited in independent claims 1, 5 and 9.

Ohki discloses a number of semiconductor device packages directed to heat dissipation. See, Abstract. Figure 22 of Ohki shows a multi-chip module **300** that includes a number of chips **232-1** to **232-4** mounted on a circuit board **231** with the chips **232-1** to **232-4** and circuit board **231** sealed in a resin package **235**. See, col. 18, lines 18-30. In order to provide heat radiating passages in the multi-chip module **300**, the circuit board **231** includes a ceramic base board **240** having a high heat conductivity coupled to a number of heat conductive blocks **234-1** to **234-4** and **101-1** to **101-4** formed of the same ceramic material as the base board **240**. See, col. 13, lines 42-48 and col. 14, lines 14-16. Ohki does not teach or suggest a semiconductor device having outer leads that include **upper electrical connecting surfaces** on the side of the upper surface of a sealing member, as recited in independent claims 1, 5 and 9.

To the contrary, Ohki is not directed to device stacking and the Ohki multi-chip module **300** includes no upper electrical connecting surfaces for outer leads whatsoever. While the Office Action asserts on page 2 that the leads **237** of Ohki's multi-chip module **300** include "upper electrical connecting surfaces on the side of the upper surface of a sealing member", a review of Fig. 22, as well as Figs. 1-21 and 23-25, show that Ohki discloses no package whatsoever having any form of upper electrical connecting surface or equivalent structure.

In comparison to the Ohki modules, the present invention provides a chip packing approach that allows for stacking of thin Quad Flat Nonlead (QFN) packages while allowing for adequate heat dissipation. See, col. 1, lines 7-11 and col. 3, lines 3-10. As Ohki does not even disclose any module useable for stacking, the Ohki modules have no need for upper electrical

connection surfaces on their outer leads and therefore disclose none. Thus, Ohki does not teach or suggest each and every limitation of the claimed invention.

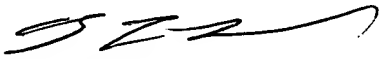
Accordingly, independent claims 1, 5 and 9 define patentable subject matter. Claims 2-4, 6-8 and 10-13 define patentable subject matter by virtue of their dependency as well as for the additional features they recite. Accordingly, withdrawal of the rejections of claims 1-13 under 35 U.S.C. §§ 102(b) and 103(a) is respectfully requested.

For the reasons given, Applicants believe that this application is in condition for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representative listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT, WILL & EMERY



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